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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,629	04/01/2004	Philippe Bienvenu	03-RO-111; B5921US; 2269-	2835

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Bryan A. Santarelli
GRAYBEAL JACKSON HALEY LLP
Suite 350
155 - 108th Avenue NE
Bellevue, WA 98004-5973

EXAMINER	
RUTLAND WALLIS, MICHAEL	

ART UNIT	PAPER NUMBER
2836	

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02/21/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,629	BIENVENU ET AL.	
	Examiner	Art Unit	
	MICHAEL RUTLAND WALLIS	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/31/2007 has been entered.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-11 and 13-20 are rejected under 35 U.S.C. 103(a) as being anticipated by Menniti (U.S. Pat. No. 4,723,191)

With respect to claims 9-10 and 17-20 Menniti teaches a circuit (Fig. 2), comprising: a switch (item T1) operable to conduct a current to a first node of a power supply (node identified as IN) when the first node has a predetermined polarity (positive) relative to a second node (lower node from node identified as IN) of the power supply; and a first delay element (delay formed with connection of trigger circuit elements Z2 and T2, see col. 4 lines 10-15) coupled to the switch (item T1) and operable to disable (reverse conduction) the switch from conducting current at a time (time set by the switching of Z2 and T2) after the polarity reverses (described as negative voltage transients). Menniti does cite the time period associated with the triggering of the trigger circuit as a predetermined time. It would have been obvious to one of ordinary skill in the art at the time of the invention to select the components of the first delay element such that period of time is short thereby limiting the time a reverse polarity is conducted.

With respect to claim 11 Menniti teaches a second delay (divider R1 and R2 combined with the regulator R) element disabling the switch (T1) in response to a normal condition of the current (col. 3 lines 40-45).

With respect to claims 13-14 and 16 Menniti teaches conducting a current between first (node identified as IN) and second supply nodes (lower node from node identified as IN) when the first node has a predetermined polarity relative to a second node; and disabling (via T1) the conducting of current at a time

after the polarity inverts. Menniti does cite the time period associated with the triggering of the trigger circuit as a predetermined time. It would have been obvious to one of ordinary skill in the art at the time of the invention to select the components of the first delay element such that period of time is short thereby limiting the time a reverse polarity is conducted.

With respect to claim 15 Menniti teaches the conducting of current is disabled in response to a normal condition of the current (col. 3 lines 40-45).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Menniti (U.S. Pat. No. 4,723,191) in view of Ngo et al. (U.S. Pat. No. 6,525,515)

With respect to claim 12 Menniti teaches the switch comprises a transistor (T1) however teaches the use of bipolar junction transistors and therefore does not teach the use of a gate terminal. Ngo teaches an under voltage lockout circuit (Fig. 2) wherein a MOSFET with a gate terminal is used to isolate the load and the supplied current Ngo further teaches gate capacitance control (col. 3 lines 40-65). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Menniti to use a MOSFET arrangement with means to discharge the gate capacitance of a gate terminal in order to implement a digital controlled regulation.

Claims 1-6 and alternatively claims 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ngo et al. (U.S. Pat. No. 6,525,515) in view of Menniti (U.S. Pat. No. 4,723,191)

With respect to claim 1, 3, 9-11, 13-16 and 17-20 Ngo teaches A device for protecting a circuit against a polarity reversal of a connection to a power

supply, the device comprising: a controllable switch (items N1 or N40) interposed on said connection between a first terminal (see first ground "-" terminal exiting supply) of a first voltage of said power supply and a first terminal of said circuit (see first terminal of pluggable system); and first means (see for example UVLO connection of controller item 44) for turning-off the switch with a turn-off delay in the presence of a under voltage; and second means (items Z1-Z3) for turning on the switch with a turn-on, when the polarity is normal (power is good). Ngo does not teach the supply is a DC supply, the under voltage is a reverse polarity or the differences in the delay times. Ngo teaches only a general power supply and not the use of a DC type supply, however the use of DC powered computer systems are well known. Ngo does not teach sensing of the polarity the voltage, Ngo only teaches the under voltage is a minimum voltage level. Menniti (col. 2 lines 10-35) teaches a negative polarity voltage level detection circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ngo to use a DC supply to power computer components which require DC input power and to set UVLO to a negative voltage level in order to reduce damage to circuit components. Ngo teaches the turn on delay associated with the second means may be programmed or set (col. 5 line 55), however makes no comparison to the delay for turning off. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ngo to program a delay (select resistance values) such that a shorter turn on delay is set in order to allow power to flow to the device quickly.

With respect to claim 2 Ngo teaches the delay associated (col. 2 lines 60-65) with turning off the passing of current is set to prevent anomalous switching due to transients.

With respect to claim 4 Ngo teaches said first means comprise a microcontroller (item 44) having an output controlling said switch.

With respect to claim 5 Ngo teaches the switch is a MOS transistor. Ngo does not teach the channel of the transistor is n-type. The use of N and P channel MOSFETs is well known to control the flow of current. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ngo to use an N channel in order to correspond to the type of logic signals sent from the controller.

With respect to claim 6 and 12 Ngo teaches a resistor connected to the gate terminal of the switch via the control terminal. Ngo further teaches an embodiment wherein a first resistor (R2) connecting the gate (see Fig. 1) of the transistor to said first terminal of the circuit to be protected. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ngo to include the use of a resistor connected to the gate in order to provide a programmable delay value.

Allowable Subject Matter

Claims 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: Ngo as modified by Menniti teach a device for protection against voltage polarity, however fails to further teach the use of a second resistor in series with a diode connects a terminal of the device connected to a second voltage of the D.C. power supply. At least this further limitation is not taught or rendered obvious by the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836

MRW